Kindly enter the following amendments:

IN THE CLAIMS:

Please amend Claims 1 - 2, 5 - 8 and 11 - 14 as follows:

1. (Once Amended) A delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level, comprising:

an inverter chain containing not less than one inverter; and

a metal-oxide-semiconductor capacitor, known as a MOS capacitor, having a single transistor per stage of the inverter chain connected to an output section of the inverter and, when a logic signal having a targeted logic level is input, changes from an off-state to an on-state during a transition period of a signal that appears in the output section of the inverter, wherein each stage is tied alternately to one of a power voltage source and a ground voltage source.

2. (Once Amended) A delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level, comprises:

an inverter chain containing not less than one inverter; and

a metal-oxide-semiconductor capacitor, known as a MOS capacitor, having a single transistor per stage of the inverter chain connected to an output section of the inverter and exhibiting changes in its capacitance to correspond with changes in output resistance of the inverter in relation to a source voltage, wherein each stage is tied alternately to one of a power voltage source and a ground voltage source.

5. (Once Amended) A delay circuit according to claim 1, wherein the MOS capacitor is a node disposed on a transmission path of a logic signal, and is at least represented by [an] a single n-MOS transistor whose gate is connected to a first node of the inverter chain that changes a logic level of the logic signal from a low level to a high level, and whose source and whose drain are fixed at a ground potential.

6. (Once Amended) A delay circuit according to claim 1, wherein the MOS capacitor is a node disposed on a transmission path of a logic signal, and is at least represented by a single p-MOS transistor whose gate is connected to a first node of the inverter chain that changes a logic level of the logic signal from a high level to a low level, and whose source and drain are fixed at a [ground] power potential.

7. (Once Amended) A delay circuit [according to claim 1] for delaying a logic signal having two logic levels consisting of a low level and a high level, comprising:

an inverter chain containing not less than one inverter; and

a metal-oxide-semiconductor capacitor, known as a MOS capacitor, connected to an output section of the inverter and, when a logic signal having a targeted logic level is input, changes from an off-state to an on-state during a transition period of a signal that appears in the output section of the inverter,

wherein the MOS capacitor is a node disposed on a transmission path of a logic signal, and is represented by an n-MOS transistor whose source and drain are connected to a node that changes a logic level of the logic signal from a high level to a low level, and whose gate is fixed at a source voltage.

8. (Once Amended) A delay circuit [according to claim 1] for delaying a logic signal having two logic levels consisting of a low level and a high level, comprising:

an inverter chain containing not less than one inverter; and

a metal-oxide-semiconductor capacitor, known as a MOS capacitor, connected to an output section of the inverter and, when a logic signal having a targeted logic level is input, changes from an off-state to an on-state during a transition period of a signal that appears in the output section of the inverter,

wherein the MOS capacitor is a node disposed on a transmission path of a logic signal, and is represented by a p-MOS transistor whose source and drain are connected to a node that changes a logic level of a logic signal from a high level to a low level, and whose gate is fixed at a ground potential.

11. (Once Amended) A delay circuit according to claim 2, wherein the MOS capacitor is a node disposed on a transmission path of a logic signal, and is at least represented by [an] a single n-MOS transistor whose gate is connected to a first node of the inverter chain that changes a logic level of the logic signal from a low level to a high level, and whose source and whose drain are fixed at a ground potential.

12. (Once Amended) A delay circuit according to claim 2, wherein the MOS capacitor is a node disposed on a transmission path of a logic signal, and is at least represented by a single p-MOS transistor whose gate is connected to a first node of the inverter chain that changes a logic level of the logic signal from a high level to a low level, and whose source and drain are fixed at a ground potential.

13. (Once Amended) A delay circuit [according to claim 2] for delaying a logic signal having two logic levels consisting of a low level and a high level, comprises:

an inverter chain containing not less than one inverter; and

a metal-oxide-semiconductor capacitor, known as a MOS capacitor, connected to an output section of the inverter and exhibiting changes in its capacitance to correspond with changes in output resistance of the inverter in relation to a source voltage,

wherein the MOS capacitor is a node disposed on a transmission path of a logic signal, and is represented by an n-MOS transistor whose source and drain are connected to a node that changes a logic level of the logic signal from a high level to a low level, and whose gate is fixed at a source voltage.